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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/533,619	03/22/2000	Angela T. Hui	1376P/D922	7885

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EXAMINER
LOUIE, WAI SING

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/533,619	Applicant(s) HUI ET AL.	
	Examiner Wai-Sing Louie	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Feldner et al. (US 6,300,235), newly cited.

With regard to claim 1, Feldner et al. disclose a method of forming metal contacts in a semiconductor device (col. 4, line 8 to col. 8, line 27 and fig. 2) comprising:

a) Providing an interlayer dielectric 418 on the lower layer (fig. 2c);

b) Providing an antireflective coating (ARC) layer 513, at least a portion of the ARC layer 513 being on the interlayer dielectric 418 (fig. 2c);

c) Providing a plurality of via holes 508 in the interlayer dielectric 418 and the ARC layer 513 (col. 1, lines 19-23);

d) Filling the plurality of via holes 508 with a conductive material (col. 1, lines 40-44);

e) Removing the ARC layer 513 (col. 6, lines 54-60). Inherently, the undesirable conductivity material in the trench and via would be removed along with the photoresist 500 and ARC 513. Feldner et al. disclose using RIE etching to remove ARC layer (col. 6, line 56).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Feldner et al. (US 6,300,235).

With regard to claim 7, Feldner et al. disclose the trench is filled with metal, which is then polished (col. 1, lines 29-32), but do not disclose a chemical mechanical polish process is used. However, the chemical mechanical polish process is well known process in the art. Therefore, it would have been obvious to use chemical mechanical polish process to polish the metal.

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feldner et al. (US 6,300,235) in view of Brooks et al. (US 5,786,276), previously used.

With regard to claims 2 and 3, Feldner et al. disclose utilizing a RIE with C_4F_8 type fluorine containing chemistry etching (col. 6, lines 54-62), but do not disclose the plasma etching with CH_3F/O_2 or CHF_3/O_2. However, Brooks et al. disclose a plasma etching process (Brooks col. 2, lines 50-54) using a mixture of methyl fluoride (CH_3F), carbon tetrafluoride (CF_4) and oxygen (O_2) to remove the ARC (Brooks col. 2, lines 57-64 and table 1A). Brooks et al. teach that it is difficult to etch silicon nitride (Brooks col. 2, lines 31-36) and Brooks et al. introduce the chemical downstream etching which is faster and selectively for nitride (Brooks col. 3, lines 20-23). Therefore, it would have been obvious to one with ordinary skill in the art to modify Feldner's method with the teaching of Brooks et al. to use CH_3F, CF_4, and O_2 mixture to dry plasma etch the ARC in order to yield faster rate.

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feldner et al. (US 6,300,235) in view of Wuu et al. (US 6,222,214), previously used.

With regard to claim 4, Feldner et al. disclose the conductive material used to fill the plurality of via holes (col. 1, lines 40-44), but do not disclose the conductivity material is tungsten. However, tungsten is a common material used to create a contact plug, such as disclosed in Wuu et al. (Wuu col. 7, lines 12-13). Therefore, it would have been obvious to use tungsten to fill the plurality of via holes.

With regard to claim 5, Feldner et al. do not disclose the interlayer dielectric is BPTEOS. However, Wuu et al. disclose a method of forming metal contacts in a semiconductor device

utilizing BPTEOS as interlayer dielectric layer (Wuu col. 6, lines 32-44). Wuu et al. teach that BPTEOS is a low flow glass and a good barrier layer (Wuu col. 6, lines 32-44). Therefore, it would have been obvious to one with ordinary skill in the art to modify Feldner's method with the teaching of Wuu to use BPTEOS as dielectric interlayer in order to apply it easily and it is good barrier layer.

With regard to claim 6, Feldner et al. disclose the device interconnected to form memory cells such as RAM, DRAM, and ROM (col. 4, lines 55-67), but do not disclose the lower layer includes memory cell fabricated on the semiconductor device. However, it is well known in the art to have memory cell on the lower layer under the interconnects such as disclosed in Wuu et al. forming SRAM cells with the interconnect metal contacts (Wuu fig. 9). Therefore, it would have been obvious to include a plurality of memory cells on the semiconductor layer in Feldner's device.

Response to Arguments

Applicant's arguments filed 3/5/03 have been fully considered but they are not persuasive.

- Applicant argues that Feldner et al. (US 6,300,235) do not disclose "removing the ARC layer while reducing subsequent undesirable charge gain and subsequent undesirable charge loss over the use of a chemical mechanical polish in removing the arc layer". However, "reducing subsequent undesirable charge gain and subsequent undesirable charge loss" is a functional language, which does not carry any patentable weight. Since applicant does not claim what type of ARC

removal process, any removal process other than CMP such as the reactive ion etching would meet the limitation. Therefore, Feldner et al. meet the limitations of claim 1.

- Applicant argues that Feldner do not disclose "where the lower layer includes a plurality of memory calls and is first layer fabricated on the semiconductor device". Feldner et al. disclose the structure could apply to a RAM, ROM, DRAM, and a SDRAM in an IC (col. 4, 55-67). However, it is common in the art to have memory cells in the semiconductor device such as Wuu. Therefore, Feldner et al. in combination with Wuu et al. would meet the limitations.
- Applicant argues that CMP process applies to a conductive layer in claim 7 is not a well-known process. However, CMP applies to a conductive layer is very common such as disclosed in Tsou et al. (US 6,265,305), Lee (US 6,300,672), Avanzino et al. (US 6,410,443), Hui et al. (US 6,506,683), and Chen (US 6,509,278). Therefore, CMP applied on a conductive layer is a well-known process.
- Applicant argues that there is no motivation to combine Feldner et al. and Brooks in the combination to perform plasma etching of ARC utilizing CH_3F/O_2 or CHF_3/O_2. However, Brooks et al. disclose plasma dry etching of ARC utilizing CH_3F/O_2 or CHF_3/O_2. Brooks et al. teach that it is difficult to etch the ARC (Brooks col. 2, lines 31-36) and Brooks et al. introduce the plasma etching which is faster and selective (Brooks col. 3, lines 20-23). Therefore, Brooks' teaching

motivates Feldner et al. to modify the etching process. The combination of Feldner with Brooks is proper.

- Applicant argues that there is no suggestion or motivation to combine Feldner et al. and Wuu et al. to fill the via holes with tungsten. However, tungsten plug is well known in the art. Wuu et al. is only an example to proof that had been done before.
- Applicant argues that Feldner et al. and Wuu et al. combine do not teach or suggest the "interlayer dielectric is BPTEOS". Wuu et al. disclose utilizing BPTEOS as interlayer dielectric layer (Wuu col. 6, lines 32-44). BPTEOS is an insulating layer, which is commonly used in the art as an interlayer insulation. Therefore, the combination of Feldner et al. and Wuu et al. is proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wai-Sing Louie whose telephone number is (703) 305-0474. The examiner can normally be reached on 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LONG PHAM
PRIMARY EXAMINER

wsl
May 18, 2003